# TDI "LDB MODE"
# System Functional Test
# Procedure

**Version 1.1**

**March 15, 2000**

Prepared by: William Mocarsky

**Signature Sheet**

Prepared By: _____Date:_____
William Mocarsky/566

Approved By:_____Date:_____
Kevin Ballou/566
TDI System Engineer

Concur: _____Date:_____
Dwayne Morgan/584
TDI Product Development Lead

**CHANGE INFORMATION PAGE**

| Version | Date | Description | Affected Pages |
|---|---|---|---|
| 1.0 | 03/06/2000 | Original. | All |
| 1.1 | 03/14/2000 | 1. Added a sentence explaining that the differences between the 2 docs are "redlines" encountered during prototype tests and a decrease in Wait times to speed up tests.<br>2. Changed all Wait 2 minutes to Wait 1 minute.<br>3. Added - " Verify A data source is FIFO", "Change B clock register to 0x00" to get the initial state of the TDI board correct. (Worked first time, but if run successively, the TDI was not properly configured).<br>4. Modified to add a wait for the bit sync to time-out and clarify which indicator to look at on the bit sync.<br>5. Modified to add a wait for the bit sync to time-out and clarify which indicator to look at on the bit sync.<br>6. Moved (starting clocks) to after step 5 (reading the registers) Changed the values to set clock registers to 0xcc.<br>7. Changed expected values of the clock registers to 0x00.<br>8. Change the expected values of the clock registers to be 0xcc.<br>9. Deleted exiting the TDI software. | 1. Page 1: section 1.0<br>2. Pages 5-17<br>3. Page 5 Section 3.3 Step 4<br>4. Page 12 Section 3.9 steps 13/14 and 16/17<br>5. Page 13 Section 3.10 steps 11/12 and 14/15<br>6. Page 17 Section 3.14<br>7. Page 17 Section 3.14 - Step 5<br>8. Page 17 Section 3.14 - step 8+11<br>9. Page 17 section 3.14 |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

## 1. Overview

This document describes the LDB Mode System Functional Test (SFT) that is to be performed on every TDI card. This version of the procedure differs from Version 1.0 in that "red-lines" encountered during the prototype testing are incorporated and the wait times are lessened to shorten the test time.

### 1.1 Test Purpose

The purpose of this test is to demonstrate that all functions of the TDI board work properly. This test will be run in ambient and during the TDI thermal tests.

### 1.2 Test Organization

This test exercises the LDB mode TDI board in the 10 configurations identified in the Ultra Long Duration Balloon (ULDB) TDRSS Data Interface (TDI) Test Plan. These modes, when coupled with the modes exercised by the ULDB System Functional Procedure, test all the circuitry within the TDI.

### 1.3 Applicable Documents

The following documents are applicable to this document:

| | |
|---|---|
| Ultra Long Duration Balloon (LDB) TDRSS Data Interface (TDI) Test Plan | December 1999 |
| Ultra Long Duration Balloon (LDB) TDRSS Data Interface (TDI) Interface Control Document | January 2000 |
| Electrostatic Discharge Control, NASA-STD-8739.7 | December 1997 |

### 1.4 Configuration Management

This document shall be managed by the ULDB TDI development team. Changes to this test procedure shall require the approval of the Ultra Long Duration (ULDB) TDRSS Data Interface (TDI) Product Development Lead.

During the execution of this test, typographical and procedural flow changes may be made at the discretion of the TDI Test Engineer. The changes will then be submitted for approval at the conclusion of the test.

After test execution, the completed test procedure shall be maintained by the TDI team as an "As Run" procedure.

### 1.5 Quality Assurance

This test will not be monitored by quality assurance. However, prior to the execution of this test, the test engineer shall verify the test configuration, test equipment calibration, documentation and ESD certification of test personnel. After this initial verification, testing shall commence. If anomalies are encountered during the execution of this test, the TDI Systems Engineer shall be notified. The execution of this test procedure shall be documented on a GSFC Work Order Authorization (WOA). Any anomalies shall be logged as a Non-Conformance Report (NCR) as per the GSFC QMS. At the conclusion of the test, the TDI Systems Engineer shall review the test results and approve any typographical changes or procedural flow deviations.

## 2. Test Setup

### 2.1 Test Personnel

This test shall be performed by one or more test conductors:

_____
Test Conductor # 1

_____
Test Conductor #2

**2.2 Documentation Required**

To commence testing, two documents shall be in place. First a signed copy of this test procedure is required. Second a GSFC WOA is in place.

This test procedure has been signed: Check_____

A GSFC WOA is in place. WOA Number:_____

If this procedure is being run as part of another procedure record Event#
Of the WOA:
EventNumber:_____ or Invoking Procedure Step Number:_____ Check:_____

**2.3 Equipment Required**

The following equipment is required for this test. Refer to the test plan for configuration details.

If this procedure is being executed as a standalone procedure ie not part of another procedure, then the following shall be verified:

| | Cal ID | Cal Date |
|---|---|---|
| PC-104 development system OR "flight like CDM" | | |
| TDI Board | | |
| Bit Sync with viterbi decoder | | |
| Firebird 6000 Communications Analyzer | _____ | _____ |
| Phillips PM6680B High Resolution Prog Timer/Counter | _____ | _____ |
| ULDB TDI "Diagnostic Software" | | |

All required calibratable test gear is in calibration Check:_____

**2.4 Test Configuration**

If this procedure is being executed as a "standalone procedure", ie not part of another procedure, then the following shall be verified.

The test set-up is configured as in Figure 2.4. Check:_____

**2.5 ESD Precautions:**

All TDI hardware shall be handled in compliance with NASA-STD-8739.7 for Electrostatic Discharge Control. All test personnel shall have current ESD certification. All test areas and benches shall also be ESD certified and test area shall be maintained between 30% and 70% humidity.

Wrist straps shall be worn at all times while either handling or within 3 feet of the TDI hardware. These wrist straps shall be verified for resistance at least 1 time each day. Non-static generating garments shall be worn by test personnel when within 3 feet of the TDI board.

If this procedure is being executed as a "standalone procedure" ie, not part of another procedure, then the following steps shall be performed.

Test facility is between 30% and 70% humidity. Check:_____

Test personnel have ESD certification. Check:_____

Wrist straps are functioning. Check:_____

Non-static generating clothing is worn. Check:_____

## 3. System Functional Test Procedure

### 3.1 Test Initialization

If this test is not part of a larger test, then

(1) Verify that the PC 104 development system or "flight like CDM" is powered off. Check:_____

(2) Verify that the TDI GSE rack is powered off. Check:_____

(3) Record the serial number of the TDI board. SN:_____ Check:_____

(4) Record the FPGA Silicon Signature Number: Sig Num:_____ Check:_____

(5) Verify that the TDI ULDB Mode select jumper is installed Check:_____

(6) Record TDI board IRQ and Base Address settings.
IRQA: _____ IRQB:_____
Base Addr:_____ Check:_____

(7) Verify that the GSE telemetry cable is connected to TDI connector P4 Check:_____

(8) Verify that the GSE test point cables are connected to TDI connectors P5 and P6 Check:_____

(9) Power the TDI GSE rack Check:_____

(10) Verify the Bit Sync Stored format settings.

a. Enter 130 on bit sync key-pad and verify
Data Rate = 3.000*10**5
Input Code = 0 (NRZ-L)
FEC Code = 2 (BPSK-D)
FEC Rate=1 (1/2)

b. Enter 131 on bit sync key-pad and verify
Data Rate = 1.500*10**5
Input Code = 0 (NRZ-L)
FEC Code = 0 (OFF)
FEC Rate= N/A

c. Enter 132 on bit sync key-pad and verify
Data Rate = 2.000*10**3
Input Code = 0 (NRZ-L)
FEC Code = 2 (BPSK-D)
FEC Rate = 1 (1/2)

d. Enter 133 on bit sync key-pad and verify
Data Rate = 1.000*10**3
Input Code = 0 (NRZ-L)
FEC Code = 0 (OFF)
FEC Rate = N/A

e. Enter 134 on bit sync key-pad and verify
Data Rate = 1.000*10**5
Input Code = 0 (NRZ-L)
FEC Code = 2 (BPSK-D)
FEC Rate = 1 (1/2)

f. Enter 135 on bit sync key-pad and verify
Data Rate = 5.000*10**4
Input Code = 0 (NRZ-L)
FEC Code = 0 (OFF)
FEC Rate = N/A

g. Enter 136 on bit sync key-pad and verify
Data Rate = 1.500*10**5
Input Code = 1(NRZ-M)
FEC Code = 0 (OFF)
FEC Rate = N/A

h. Enter 137 on bit sync key-pad and verify
Data Rate = 1.500*10**5
Input Code = 3 (BiO-L)
FEC Rate = 0 (OFF)
FEC Rate = N/A

Check:_____

(11) Power the PC 104 development system or the "flight-like CDM" Check:_____

(12) Start the TDI diagnostic software Check:_____
Verify FIFO LOAD MODE = Normal
Verify MISSION MODE=LDB
If different, toggle the input to get the above settings

### 3.2 Hard Rest Verification Test

If this procedure is not being executed as a standalone procedure, but rather as part of a larger procedure which call for the execution of the SFT, then the following steps shall be performed:

(1) Read all registers and confirm their proper states at power up:
a. Read I/O Port 0x00 and confirm = 0x00. Value read:_____
b. Read I/O Port 0x01 and confirm = 0x09(A&B empty) Value read:_____
c. Read I/O Port 0x02 and confrim = 0x00(A Clock OFF) Value read:_____
d. Read I/O Port 0x03 and confirm = 0x00(A Enc Data) Value read:_____

e. Read I/O Port 0x08 and confirm = 0x00 Value read:_____
f. Read I/O Port 0x09 and confirm = 0x09(A&B empty) Value read:_____
g. Read I/O port 0x0A and confirm = 0x00 (B Clock OFF) Value read:_____
h. Read I/O Port 0x0B and confirm = 0x00(B Enc Data) Value read:_____
i. Read I/O Port 0x0F and confirm = 0x00 (A RealTime) Value read:_____

If any of the values read differ from the expected values, then the test fails: Check:_____
Circle:PASS/FAIL

**3.3 Real Time FIFO Data Processor A 150Khz Encoded Test**

(1) Enter 130 on bit sync key pad to configure bit sync as follows:
Data Rate:300Kbps(Symbol Rate)
Input Code:NRZ-L
FEC Code:BPSK-D
Rate: ½
Check:_____

(2) Configure FIREBIRD 6000 for BERT Pattern 511 and press RESTART Check:_____

(3) Patch A1TLM to BS#1 S0 IN. Check:_____

(4) Select FLOW DATA option of the Diagnostic software
Enter:BERT9.BIN for FIFO A file name
Enter:BERT6.BIN for FIFO B file name
Verify A Data Source is FIFO. If not toggle to get this setting.
Verify A ENCODING is ENCODED. If not toggle to get this setting.
Verify LDB MODE is REALTIME. If not toggle to get this setting.
Verify LDB Stream is A. If not toggle to get this setting.
Change A Clock Register to 0x28.
Change B Clock Register to 0x00.
Check:_____

(5) Wait 1 minute Check:_____

(6) Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO,
BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(7) Patch A2TLM to BS#1 S0 IN. Check:_____

(8) Press RESTART on FIREBIRD 6000. Check:_____

(9) Wait 1 minute Check:_____

(10)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO,
BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(11)Patch B1TLM to BS#1 S0 IN. Check:_____

(12)Press RESTART on FIREBIRD 6000. Check:_____

(13)Wait 1 minute Check:_____

(14)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(15)Patch B2TLM to BS#1 S0 IN. Check:_____

(16)Press RESTART on FIREBIRD 6000. Check:_____

(17)Wait 1 minute Check:_____

(18)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

### 3.4 Real Time BERT Data Processor A 150Khz Unencoded Test

(1) Enter 131 on bit sync key pad to configure bit sync as follows:
Data Rate:150Kbps(Bit Rate)
Input Code:NRZ-L
FEC Code:OFF
Rate: ½
Check:_____

(2) Configure FIREBIRD 6000 for BERT Pattern 2047 and press RESTART Check:_____

(3) Patch A1TLM to BS#1 S0 IN. Check:_____

(4) Using the Diagnostic Software,
Toggle A Data Source to BERT.
Toggle A Data Encoding to RAW
Check:_____

(5) Press RESTART on FIREBIRD 6000 Check:_____

(6) Wait 1 minute. Check:_____

(7) Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(8) Patch A2TLM to BS#1 S0 IN. Check:_____

(9) Press RESTART on FIREBIRD 6000. Check:_____

(10)Wait 1 minute. Check:_____

(11)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(12)Patch B1TLM to BS#1 S0 IN. Check:_____

(13)Press RESTART on FIREBIRD 6000. Check:_____

(14)Wait 1 minute. Check:_____

(15)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO,
BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(16)Patch B2TLM to BS#1 S0 IN. Check:_____

(17)Press RESTART on FIREBIRD 6000. Check:_____

(18)Wait 1 minute. Check:_____

(19)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO,
BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

### 3.5 Real Time FIFO Data Processor B 150Khz Unencoded Test

(1) Configure FIREBIRD 6000 for BERT Pattern 63 and press RESTART Check:_____

(2) Patch A1TLM to BS#1 S0 IN. Check:_____

(3) Using the Diagnostic Software:
If necessary, toggle B Data Source to FIFO
If necessary, toggle B Data Encoding to RAW
Toggle LDB Stream to B
Change B Clock register to 0x28
. Check:_____

(4) Press RESTART on FIREBIRD 6000 Check:_____

(5) Wait 1 minute. Check:_____

(6) Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO,
BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(7) Patch A2TLM to BS#1 S0 IN. Check:_____

(8) Press RESTART on FIREBIRD 6000. Check:_____

(9) Wait 1 minute. Check:_____

(10)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO,
BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(11)Patch B1TLM to BS#1 S0 IN. Check:_____

(12)Press RESTART on FIREBIRD 6000. Check:_____

(13)Wait 1 minute . ****. Check:_____

(14)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO,
BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(15)Patch B2TLM to BS#1 S0 IN. Check:_____

(16)Press RESTART on FIREBIRD 6000. Check:_____

(17)Wait 1 minute. Check:_____

(18)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

**3.6 Real Time BERT Data Processor B 150Khz Encoded Test**

(1) Enter130 on bit sync key pad to configure bit sync as follows:
Data Rate:300Kbps(Symbol Rate)
Input Code:NRZ-L
FEC Code: BPSK-D
Rate: ½
Check:_____

(2) Configure FIREBIRD 6000 for BERT Pattern 2047 and press RESTART Check:_____

(3) Patch A1TLM to BS#1 S0 IN. Check:_____

(4) Using the Diagnostic Software,
Toggle B Data Source to BERT.
Toggle B Data Encoding to ENCODED
Check:_____

(5) Press RESTART on FIREBIRD 6000 Check:_____

(6) Wait 1 minute. Check:_____

(7) Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(8) Patch A2TLM to BS#1 S0 IN. Check:_____

(9) Press RESTART on FIREBIRD 6000. Check:_____

(10)Wait 1 minute. Check:_____

(11)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(12)Patch B1TLM to BS#1 S0 IN. Check:_____

(13)Press RESTART on FIREBIRD 6000. Check:_____

(14)Wait 1 minute. Check:_____

(15)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(16)Patch B2TLM to BS#1 S0 IN. Check:_____

(17)Press RESTART on FIREBIRD 6000. Check:_____

(18)Wait 1 minute. Check:_____

(19)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

### 3.7 Playback Test 1 Using FIFOs as Data Source

In this section, TDI Board is placed in playback mode with both streams generating encoded FIFO data. The A stream is at 150Kbps (300Ksymbols/Sec) and the B stream is at 1Kbps (2Ksymbols/sec).

(1) Enter 130 on bit sync key pad to configure bit sync as follows:
Data Rate:300Kbps(Symbol Rate)
Input Code:NRZ-L
FEC Code:BPSK-D
Rate: ½
Check:_____

(2) Configure FIREBIRD 6000 for BERT Pattern 511 and press RESTART Check:_____

(3) Patch A1TLM to BS#1 S0 IN. Check:_____

(4) Using the Diagnostic Software,
Toggle LDB Mode to PLAYBACK
Toggle A Data Source to FIFO
Toggle A Data Encoding to ENCODED
Set A Clock Register to 0x28
Toggle B Data Source to FIFO
ToggleB Data Encoding to ENCODED
Set B Clock Register to 0xC6
Check:_____

(5) Press RESTART on FIREBIRD 6000 Check:_____

(6) Wait 1 minute. Check:_____

(7) Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(8) Patch A2TLM to BS#1 S0 IN. Check:_____

(9) Press RESTART on FIREBIRD 6000. Check:_____

(10)Wait 1 minute. Check:_____

(11)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(12)Patch B1TLM to BS#1 S0 IN. Check:_____

(13)Enter 132 on bit sync key pad to configure bit sync as follows:
Data Rate:2Kbps(Symbol Rate)
Input Code:NRZ-L
FEC Code:BPSK-D
Rate: ½
Check:_____

(14)Select Pattern 63 on FIREBIRD 6000 and press RESTART. Check:_____

(15)Wait 1 minute. Check:_____

(16)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(17)Patch B2TLM to BS#1 S0 IN. Check:_____

(18)Press RESTART on FIREBIRD 6000. Check:_____

(19)Wait 1 minute. Check:_____

(20)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

### 3.8 Playback Test 2 Using FIFOs as Data Source

In this test the TDI board configured as in Section 3.7 except the clock rates are swapped.

(1) Configure FIREBIRD 6000 for BERT Pattern 511 and press RESTART Check:_____

(2) Patch A1TLM to BS#1 S0 IN. Check:_____

(3) Using the Diagnostic Software,
Set A Clock Register to 0xC6
Set B Clock Register to 0x28
Check:_____

(4) Press RESTART on FIREBIRD 6000 Check:_____

(5) Wait 1 minute. Check:_____

(6) Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(7) Patch A2TLM to BS#1 S0 IN. Check:_____

(8) Press RESTART on FIREBIRD 6000. Check:_____

(9) Wait 1 minute. Check:_____

(10)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____ Circle:PASS/FAIL

(11)Patch B1TLM to BS#1 S0 IN. Check:_____

(12)Enter 130 on bit sync key pad to configure bit sync as follows:
Data Rate:300Kbps(Symbol Rate)
Input Code:NRZ-L
FEC Code:BPSK-D
Rate: ½
Check:_____

(13)Select Pattern 63 on FIREBIRD 6000 and press RESTART. Check:_____

(14)Wait 1 minute. Check:_____

(15)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____ Circle:PASS/FAIL

(16)Patch B2TLM to BS#1 S0 IN. Check:_____

(17)Press RESTART on FIREBIRD 6000. Check:_____

(18)Wait 1 minute. Check:_____

(19)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____ Circle:PASS/FAIL

### 3.9 Playback Test 3 Using BERT as Data Source

In this section, the TDI is in Playback mode with the A data stream generating onboard unencoded BERT data and the B data stream OFF (no clock).

(1) Enter 131 on bit sync key pad to configure bit sync as follows:
Data Rate:150Kbps(Bit Rate)
Input Code:NRZ-L
FEC Code:OFF
Rate: ½
Check:_____

(2) Configure FIREBIRD 6000 for BERT Pattern 2047 and press RESTART Check:_____

(3) Patch A1TLM to BS#1 S0 IN. Check:_____

(4) Using the Diagnostic Software,
Toggle A Data Source to BERT
Toggle A Data Encoding to RAW
Set B Clock Rate to 0x00

Set A Clock Rate to 0x28
Check:_____

(5) Press RESTART on FIREBIRD 6000 Check:_____

(6) Wait 1 minute. Check:_____

(7) Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(8) Patch A2TLM to BS#1 S0 IN. Check:_____

(9) Press RESTART on FIREBIRD 6000. Check:_____

(10)Wait 1 minute. Check:_____

(11)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(12)Patch B1TLM to BS#1 S0 IN. Check:_____

(13)Wait 20 seconds. Check:_____

(14)Verify Bit Sync "Signal Level In Range" light is not lit. If lit, test FAILS. Check:_____
Circle:PASS/FAIL

(15)Patch B2TLM to BS#1 S0 IN. Check:_____

(16)Wait 20 seconds. Check:_____

(17)Verify Bit Sync "Signal Level In Range" light is not lit. If lit, the test FAILS. Check:_____
Circle:PASS/FAIL

### 3.10 Playback Test 4 Using BERT as Data Source

In this section, the TDI is in Playback mode with the B data stream generating onboard unencoded BERT data and the A data stream OFF (no clock).

(1) Patch B2TLM to BS#1 S0 IN. Check:_____

(2) Using the Diagnostic Software,
Toggle B Data Source to BERT
Toggle B Data Encoding to RAW
Set A Clock Register to 0x00
Set B Clock Register to 0x28
Check:_____

(3) Press RESTART on FIREBIRD 6000 Check:_____

(4) Wait 1 minute. Check:_____

(5) Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(6) Patch B1TLM to BS#1 S0 IN. Check:_____

(7) Press RESTART on FIREBIRD 6000. Check:_____

(8) Wait 1 minute. Check:_____

(9) Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(10)Patch A1TLM to BS#1 S0 IN. Check:_____

(11)Wait 20 seconds. Check:_____

(12)Verify Bit Sync "Signal Level In Range" light is not lit. If lit, test FAILS. Check:_____
Circle:PASS/FAIL

(13)Patch A2TLM to BS#1 S0 IN. Check:_____

(14)Wait 20 seconds. Check:_____

(15)Verify Bit Sync "Signal Level In Range" light is not lit. If lit, the test FAILS.
Check:_____
Circle:PASS/FAIL

### 3.11 Playback Test 5 Using FIFOs as Data Source – Intermediate Data Rate

In this section, both streams of the TDI mode output encoded FIFO data. The A stream is tested at 100Ksymbols/sec and the B stream is tested at 300Ksymbols/sec.

(1) Enter 134 on bit sync key pad to configure bit sync as follows:
Data Rate:100Kbps(Symbol Rate)
Input Code:NRZ-L
FEC Code:BPSK-D
Rate: ½
Check:_____

(2) Configure FIREBIRD 6000 for BERT pattern 511 and press RESTART. Cgeck:_____

(3) Patch A1TLM to BS#1 S0 IN. Check:_____

(4) Using the Diagnostic Software,
Toggle A Data Source to FIFO
Toggle A Data Encoding to ENCODED
Toggle B Data Source to FIFO
Toggle B Data Encoding to ENCODED
Set A Clock Register to 0x4C
Set B Clock Register to 0x28
Check:_____

(5) Press RESTART on FIREBIRD 6000 Check:_____

(6) Wait 1 minute. Check:_____

(7) Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(8) Patch A2TLM to BS#1 S0 IN. Check:_____

(9) Press RESTART on FIREBIRD 6000. Check:_____

(10)Wait 1 minute. Check:_____

(11)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(12)Enter 130 on bit sync key pad to configure bit sync as follows:
Data Rate:300Kbps(Symbol Rate)
Input Code:NRZ-L
FEC Code:BPSK-D
Rate: ½
Check:_____

(13)Patch B1TLM to BS#1 S0 IN. Check:_____

(14)Configure FIREBIRD 6000 for BERT pattern 63 and press RESTART. Cgeck:_____

(15)Wait 1 minute. Check:_____

(16)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(17)Patch B2TLM to BS#1 S0 IN. Check:_____

(18)Press RESTART on FIREBIRD 6000. Check:_____

(19)Wait 1 minute. Check:_____

(20)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

### 3.12Playback Test 6 – TDI Stress Test

In this section the TDI is operated in playback mode with both channels outputting encoded FIFO data at 300Ksymbols/sec.

(21)Enter 130 on bit sync key pad to configure bit sync as follows:
Data Rate:300Kbps(Symbol Rate)
Input Code:NRZ-L
FEC Code:BPSK-D
Rate: ½
Check:_____

(22)Configure FIREBIRD 6000 for BERT pattern 511 and press RESTART. Cgeck:_____

(23)Patch A1TLM to BS#1 S0 IN. Check:_____

(24)Using the Diagnostic Software,
Set A Clock Register to 0x28
Check:_____

(25)Press RESTART on FIREBIRD 6000 Check:_____

(26)Wait 1 minute. Check:_____

(27)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO,
BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(28)Patch A2TLM to BS#1 S0 IN. Check:_____

(29)Press RESTART on FIREBIRD 6000. Check:_____

(30)Wait 1 minute. Check:_____

(31)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO,
BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(32)Patch B1TLM to BS#1 S0 IN. Check:_____

(33)Configure FIREBIRD 6000 for BERT pattern 63 and press RESTART. Cgeck:_____

(34)Wait 1 minute. Check:_____

(35)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO,
BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

(36)Patch B2TLM to BS#1 S0 IN. Check:_____

(37)Press RESTART on FIREBIRD 6000. Check:_____

(38)Wait 1 minute Check:_____

(39)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO,
BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____
Circle:PASS/FAIL

**3.13Test TDI Test Points**

(1) Enter 136 on bit sync key pad to configure bit sync as follows:
Data Rate:150Kbps(Bit Rate)
Input Code:NRZ-M
FEC Code:OFF
Rate: ½
Check:_____

(2) Configure FIREBIRD 6000 for BERT pattern 511 and press RESTART. Cgeck:_____

(3) Patch NRZ-M A TP to BS#1 S0 IN. Check:_____

(4) Press RESTART on FIREBIRD 6000. Check:_____

(5) Wait 1 minute. Check:_____

(6) Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____ Circle:PASS/FAIL

(7) Patch NRZ-M B TP to BS#1 S0 IN Check:_____

(8) Configure FIREBIRD 6000 for BERT pattern 63 and press RESTART. Check:_____

(9) Wait 1 minute. Check:_____

(10)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____ Circle:PASS/FAIL

(11)Enter 137 on bit sync key pad to configure bit sync as follows:
Data Rate:150Kbps(Bit Rate)
Input Code:BiO-L
FEC Code:OFF
Rate: ½

(12)Patch BiO-L A TP to BS#1 S0 IN Check:_____

(13)Configure FIREBIRD 6000 for BERT pattern 511 and press RESTART. Check:_____

(14)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____ Circle:PASS/FAIL

(15)Patch BiO-L B TP to BS#1 S0 IN Check:_____

(16)Configure FIREBIRD 6000 for BERT pattern 63 and press RESTART. Check:_____

(17)Wait 1 minute . Check:_____

(18)Record: Bit Errors:_____ BLOCKS:_____. If Bit errors is NON ZERO, BLOCK is ZERO or SYNC LOST light ON, then test FAILED. Check:_____ Circle:PASS/FAIL

(19)Patch A1xCLK to frequency counter. Verify the counter reads 150000 +/- 150 counts. Record Counts:_____ Check:_____

(20)Patch A2xCLK to frequency counter. Verify counter reads 300000 +/- 300 counts. Record Counts:_____ Check:_____

(21)Patch B1xCLK to frequency counter. Verify counter reads 150000 +/- 150 counts. Record Counts:_____ Check:_____

(22)Patch B2xCLK to frequency counter. Verify counter reads 300000 +/- 300 counts. Record Counts:_____ Check:_____

(23)Exit the FLOW DATA section of the Diagnostic Software. Check:_____

**3.14Test TDI Soft Reset Test**

(1) Issue SOFT Resets to A and B sides and disable clocks
Write to I/O Port 0x01 the value 0x00
Write to I/O Port 0x09 the value 0x00
Write to I/O Port 0x02 the value 0x00
Write to I/O Port 0X0A the value of 0x00

Check:_____

(2) Set the A side of the TDI board in BERT Encoded mode and the B side of the TDI board in the BERT Unencoded Mode
Write to I/O Port 0x03 the value 0x01
Write to I/O Port 0x0B the value 0x03

Check:_____.

(3) Set TDI LDB Mode Configuration register to PLAYBACK Mode, LDB Stream B.
Write I/O Port 0x0F the value 0x03

Check:_____

(4) Fill both the A and B FIFOs with any pattern by:
Select FILL FIFO
Enter 65536 for the fill count.
Enter 0xAA for the data pattern
Enter 3 to select BOTH FIFOs

Check:_____

(5) Verify register contents as follows:

| | |
|---|---|
| Read I/O Port 0x00 (FIFO A LATCHED) | Exp Value=0xA4 Rec Value:_____ |
| Read I/O Port 0x01 (FIFO A Unlatched) | Exp Value=0xB6 Rec Value:_____ |
| Read I/O Port 0x02 (A Clock) | Exp Value=0x00 Rec Value:_____ |
| Read I/O Port 0x03(A Config Register) | Exp Value=0x01 Rec Value:_____ |
| Read I/O Port 0x08 (FIFO B LATCHED) | Exp Value=0xA4 Rec Value:_____ |
| Read I/O Port 0x09 (FIFO B Unlatehed) | Exp Value=0xB6 Rec Value:_____ |
| Read I/O Port 0x0A (B Clock) | Exp Value=0x00 Rec Value:_____ |
| Read I/O Port 0x0B (B Config Register) | Exp Value=0x03 Rec Value:_____ |
| Read I/O Port 0x0F (LDB Mode Config) | Exp Value=0x03 Rec Value:_____ |

If any of the read values differ from the expected value the test FAILED.

Check:_____
Circle:PASS/FAIL

(6) Start both clocks
Write to I/O Port 0x02 the value 0xCC
Write to I/O Port 0x0A the value 0xCC

Check:_____

(7) Write to I/O Port 01 the value 0x00 (A SOFT RESET) Check:_____

(8) Verify only the A FIFO reset to empty by reading the following registers:

| | |
|---|---|
| Read I/O Port 0x00 (FIFO A LATCHED). | Exp Value=0xA0. Rec Value:_____ |
| Read I/O Port 0x01 (FIFO A UNLATCHED) | Exp Value=0xB1 Rec Value:_____ |
| Read I/O Port 0x02 (A Clock) | Exp Value=0xCC Rec Value:_____ |

| | |
|---|---|
| Read I/O Port 0x03(A Config) | Exp Value=0x01 Rec Value:_____ |
| Read I/O Port 0x08 (FIFO B LATCHED). | Exp Value=0xA0. Rec Value:_____ |
| Read I/O Port 0x09 (FIFO B UNLATCHED) | Exp Value=0xB1 Rec Value:_____ |
| Read I/O Port 0x0A (B Clock) | Exp Value=0xCC Rec Value:_____ |
| Read I/O Port 0x0B (B Config) | Exp Value=0x03 Rec Value:_____ |
| Read I/O Port 0x0F (LDB Mode Conf) | Exp Value=0x03 Rec Value:_____ |

If any differences, the test FAILED. Check:_____
Circle:PASS/FAIL

(9) Write to I/O Port 0x00 the value 0x01 (Any data in FIFO A) Check:_____

(10)Write to I/O Port 0x09 the value of 0x00 (B SOFT RESET) Check:_____

(11)Verify only the B FIFO emptied bits by reading the following registers:

| | |
|---|---|
| Read I/O Port 0x00 (FIFO A LATCHED). | Exp Value=0x80. Rec Value:_____ |
| Read I/O Port 0x01 (FIFO A UNLATCHED) | Exp Value=0x88 Rec Value:_____ |
| Read I/O Port 0x02 (A Clock) | Exp Value=0xCC Rec Value:_____ |
| Read I/O Port 0x03(A Config) | Exp Value=0x01 Rec Value:_____ |
| Read I/O Port 0x08 (FIFO B LATCHED). | Exp Value=0x80. Rec Value:_____ |
| Read I/O Port 0x09 (FIFO B UNLATCHED) | Exp Value=0x88 Rec Value:_____ |
| Read I/O Port 0x0A (B Clock) | Exp Value=0xCC Rec Value:_____ |
| Read I/O Port 0x0B (B Config) | Exp Value=0x03 Rec Value:_____ |
| Read I/O Port 0x0F (LDB Mode Conf) | Exp Value=0x03 Rec Value:_____ |

If any differences, the test FAILED. Check:_____
Circle:PASS/FAIL

(12)Stop all clocks by writing
I/O Port 0x02 -> 0x00
I/O Port 0x0A ->0x00

Check:_____

**4. Declaration of Test Results**

If there where no failures encountered during the execution of this test procedure that were not induced by procedural errors or GSE failures, then the TDI board in LDB mode PASSES the TDI LDB MODE SFT.

The test conductors and TDI system engineer declare that:

TDI board Serial Number:_____
FPGA Signature Number:_____

PASSED/FAILED(Circle One) the TDI LDB MODE SFT on _____(date)

Test Conductor #1_____

Test Conductor #2_____

TDI Systems Engineer:_____

# Figure 2.4 System Functional Test Configuration